

<b>INFORMATION DISCLOSURE CITATION</b> <i>(Use several sheets if necessary)</i>				Docket Number (Optional) <b>51889/2</b>		Application Number <b>10/613,169</b>	
				Applicant(s) <b>Douglas R. Hackler, Sr. et al.</b>			
				Filing Date <b>July 3, 2003</b>		Group Art Unit <b>2811</b>	
				<b>U.S. PATENT DOCUMENTS</b>			
EXAMINER INITIALS	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
PC	A1	2003/0058001	03/27/03	Boerstler et al.	326	113	09/27/01
	A2	2002/0180486	12/05/02	Yamashita et al.	326	113	06/25/02
	A3	2002/0084803	07/04/02	Mathew et al.	326	113	12/29/00
	A4	2002/0081808	06/27/02	Forbes	438	283	01/25/02
'	A5	2002/0047727	04/25/02	Mizuno	326	113	10/18/01
	A6	2001/0022521	09/20/01	Sasaki et al.	326	113	05/21/01
	A7	6,433,609	08/13/02	Voldman	327	313	11/19/01
	A8	6,420,905	07/16/02	Davis et al.	326	113	09/07/00
	A9	6,404,237	06/11/02	Mathew et al.	326	113	12/29/00
	A10	6,376,317	04/23/02	Forbes et al.	438	283	06/28/00
PC	A11	6,188,243	02/13/01	Liu et al.	326	81	06/09/99
<b>FOREIGN PATENT DOCUMENTS</b>							
REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
						YES	NO
<b>OTHER DOCUMENTS</b> <i>(Including Author, Title, Date, Pertinent Pages, Etc.)</i>							
EXAMINER <i>PHAT X. CAO</i>				DATE CONSIDERED <i>3/14/05</i>			
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FORM PTO-1449  
(REV. 7-80)U.S. DEPARTMENT OF COMMERCE  
PATENT AND TRADEMARK OFFICEATTY. DOCKET NO.  
51889/2 USAPPLICATION NO.  
10/613,169

## INFORMATION DISCLOSURE CITATION

Title: MULTI-CONFIGURABLE INDEPENDENTLY  
MULTI-GATED MOSFET

APPLICANT - Douglas R. Hackler, Sr. et al.

FILING DATE-  
July 3, 2003

## U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
PC	1	2002/0187610 A1	12/12/02	Furukawa et al.	438	283	06/12/01
	2	2002/0153587 A1	10/24/02	Adkisson et al.	257	510	07/02/02
	3	2002/0140039 A1	10/03/02	Adkisson et al.	257	377	06/18/02
	4	2002/0105039 A1	08/08/02	Hanafi et al.	257	401	02/07/01
	5	2002/0093053 A1	07/18/02	Chan et al.	257	347	01/18/02
	6	2003/0089930 A1	05/15/03	Zhao	257	256	11/07/02
	7	6,580,137 B2	06/17/03	Parke	257	401	08/29/01
	8	6,518,127 B2	02/11/03	Hshieh et al.	438	270	06/01/01
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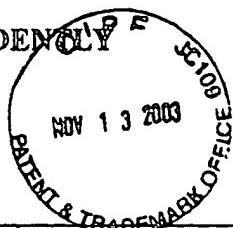
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PC	18	5,273,921	12/28/93	Neudeck et al.	437	41	12/27/91
PC	19	3,755,012	08/28/73	George et al.	148	175	03/19/71

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		DOCUMENT NUMBER	PUBLICATION DATE	COUNTRY / PATENT OFFICE	CLASS	SUBCLASS	TRANSLATION	
							YES	NO
	20							
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## OTHER DOCUMENTS (Including Author, Title, Date, Relevant Pages, Place of Publication , etc.)

PC	28	Harada et al., "2-GHz RF Front-End Circuits in CMOS/SIMOX Operating at an Extremely Low Voltage of 0.5 V," IEEE Journal of Solid-State Circuits, Vol. 35, No. 12, December 2000, pgs. 2000-2004.
PC	29	Wann et al., "CMOS with Active Well Bias for Low-Power and RF/Analog Applications," 2000 Symposium on VLSI Technology Digest of Technical Papers, 2 pgs.
PC	30	Yang et al., "Back-Gated CMOS on SOIAS for Dynamic Threshold Voltage Control," IEEE Transactions on Electron Devices, Vol. 44, No. 5, May 1997, pgs. 822-831.
PC	31	Assaderaghi et al., "Dynamic Threshold-Voltage MOSFET (DTMOS) for Ultra-Low Voltage VLSI," IEEE Transactions on Electron Devices, Vol. 44, No. 3, March 1997, pgs. 414-422.

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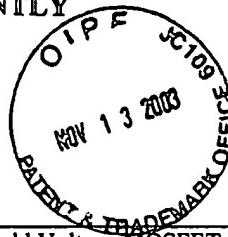
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	34	Hsu et al., "Low-Frequency Noise Properties of Dynamic-Threshold (DT) MOSFET's," IEEE Electron Device Letters, Vol. 20, No. 10, October 1999, pgs. 532-534.
	35	Wong, H.-S. Philip, "Field Effect Transistors – From Silicon MOSFETS to Carbon Nanotube FETs," Proc. 23 <sup>rd</sup> International Conference on Microelectronics (Miel 2002), Vol. 1, NIS, Yugoslavia, 12-15 May, 2002, pgs. 103-107.
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	39	Choi et al., "Nanoscale Ultrathin Body PMOSFETs With Raised Selective Germanium Source/Drain," IEEE Electron Device Letters, Vol. 22, No. 9, September 2001, pgs. 447-448.
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	44	Hokazono et al., "14 nm Gate Length CMOSFETs Utilizing Low Thermal Budget Process with Poly-SiGe and Ni Salicide," SoC Research & Development Center, Process & Manufacturing Engineering Center, System LSI Division, Toshiba Corporation Semiconductor Company, 8 Shinsugita-cho, Isogo-ku, Yokohama, Kanagawa 235-8522, Japan, pgs. 27.1.1-27.1.4.
	45	Schulz et al., "50-nm Vertical Sidewall Transistors With High Channel Doping Concentrations," Infineon Technologies AG, Corporate Research, D-81730 Munich, Germany, pgs. 3.5.1-3.5.4.
PC	46	Fung et al., "Gate length scaling accelerated to 30nm regime using ultra-thin film PD-SOI Technology," IBM Microelectronics Semiconductor Research and Development Center (SRDC), pgs. 29.3.1-29.3.4.

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PC	47	Narasimha et al., "High Performance Sub-40nm CMOS Devices on SOI for the 70nm Technology Node," IBM Microelectronics Semiconductor Research and Development Center (SRDC), Hopewell Junction, NY 12533, USA, pgs. 29.2.1-29.2.4.
PC	48	Hisamoto, Digh, "FD/DG-SOI MOSFET - a viable approach to overcoming the device scaling limit," Central Research Laboratory, Hitachi Ltd., Kokubunji, Tokyo 185-8601, Japan, pgs. 19.3.1-19.3.4.
	49	Kedzierski et al., "Complementary silicide source/drain thin-body MOSFETs for the 20nm gate length regime," Department of Electrical Engineering and Computer Sciences, University of California at Berkeley, Berkeley, CA, 94720, USA, pgs. 3.4.1-3.4.4.
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	52	Tavel et al., "High Performance 40nm nMOSFETs With HfO <sub>2</sub> Gate Dielectric and Polysilicon Damascene Gate," France Telecom R&D, B.P. 98, 38243 Meylan, France, pgs. 17.1.1-17.1.4.
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	54	Monfray et al., "SON (Silicon-On-Nothing) P-MOSFETs with totally silicided (CoSi <sub>2</sub> ) Polysilicon on 5nm-thick Si-films: The simplest way to integration of Metal Gates on thin FD channels," ST Microelectronics, 850, rue J.Monnet, 38921 Crolles, France, pgs. 10.5.1-10.5.4.
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	56	Wong et al., "Design and Performance Considerations for Sub-0.1 $\mu\text{m}$ Double-Gate SOI MOSFET's," I.B.M. Thomas J. Watson Research Center, P.O. Box 218, Yorktown Heights, New York 10598, U.S.A., pgs. 30.6.1-30.6.4.
	57	Wong et al., "Device Design Considerations for Double-Gate, Ground-Plane, and Single-Gated Ultra-Thin SOI MOSFET's at the 25 nm Channel Length Generation," IBM T.J. Watson Research Center, P.O. Box 218, Yorktown Heights, New York 10598, U.S.A., pgs. 15.2.1-15.2.4.
	58	Guarini et al., "Triple-Self-Aligned, Planar Double-Gate MOSFETs: Devices and Circuits," IBM T.J. Watson Research Center, Yorktown Heights, New York 10598, U.S.A., pgs. 19.2.1-19.2.4.
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PC	61	Oh et al., "Analytic Description of Short-Channel Effects in Fully-Depleted Double-Gate and Cylindrical, Surrounding-Gate MOSFETs," IEEE Electron Device Letters, Vol. 21, No. 9, September 2000, pgs. 445-447.

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	66	Samavedam et al., "Dual-Metal Gate CMOS with HfO <sub>2</sub> Gate Dielectric," Motorola Digital DNA™ Laboratories, 3501 Ed Bluestein Blvd., MD:K10, (*AMD), Austin, TX 78721, USA, pgs. 17.2.1-17.2.4.
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PC	74	Ducroquet et al., "Full CMP Integration of CVD TiN Damascene Sub-0.1-μm Metal Gate Devices For ULSI Applications," IEEE Transactions on Electron Devices, Vol. 48, No. 8, August 2001, pgs. 1816-1821.

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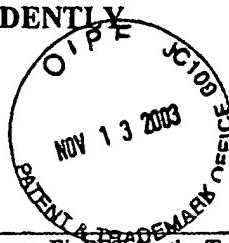
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PL	75	Choi et al., "Nanoscale CMOS Spacer FinFET for the Terabit Era," IEEE Electron Device Letters, Vol. 23, No. 1, January 2002, pgs. 25-27.
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	77	Choi et al., "A Spacer Patterning Technology for Nanoscale CMOS," IEEE Transactions on Electron Devices, Vol. 49, No. 3, March 2002, pgs. 436-441.
	78	Li et al., "Damascene W/TiN Gate MOSFETs With Improved Performance for 0.1- $\mu$ m Regime," IEEE Transactions on Electron Devices, Vol. 49, No. 11, November 2002, pgs. 1891-1896.
	79	Huang et al., "Sub-50 nm P-Channel FinFET," IEEE Transactions on Electron Devices, Vol. 48, No. 5, May 2001, pgs. 880-886.
	80	Pei et al., "FinFET Design Considerations Based on 3-D Simulation and Analytical Modeling," IEEE Transactions on Electron Devices, Vol. 49, No. 8, August 2002, pgs. 1411-1419.
	81	Hisamoto et al., "FinFET—A Self-Aligned Double-Gate MOSFET Scalable to 20 nm," IEEE Transactions on Electron Devices, Vol. 47, No. 12, December 2000, pgs. 2320-2325.
	82	Chang et al., "FinFET Scaling to 10nm Gate Length," Strategic Technology, Advanced Micro Devices, Inc., Sunnyvale, CA 94088, USA, pgs. 10.2.1-10.2.4
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	84	Lindert et al., "Sub-60-nm Quasi-Planar FinFETs Fabricated Using a Simplified Process," IEEE Electron Device Letters, Vol. 22, No. 10, October 2001, pgs. 487-489.
	85	Huang et al., "Sub 50-nm FinFET: PMOS," Department of Electrical Engineering and Computer Sciences, University of California at Berkeley, CA 94720, USA, pgs. 3.4.1-3.4.4.
	86	Choi et al., "Sub-20nm CMOS FinFET Technologies," Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, CA 94720, USA, pgs. 19.1.1-19.1.4.
	87	Kedzierski et al., "Metal-gate FinFET and fully-depleted SOI devices using total gate silicidation," IBM Semiconductor Research and Development Center (SRDC), Research Division, T J Watson Research Center, Yorktown Heights, NY 10598, pgs. 10.1.1-10.1.4.
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	89	Lee et al., "Hydrogen Annealing Effect on DC and Low-Frequency Noise Characteristics in CMOS FinFETs," IEEE Electron Device Letters, Vol. 24, No. 3, March 2003, pgs. 186-188.
	90	Yagishita et al., "High Performance Metal Gate MOSFETs Fabricated by CMP for 0.1 $\mu$ m Regime," Microelectronics Engineering Laboratory, Toshiba Corporation, 8, Shinsugita-cho, Isogo-ku, Yokohama 235-8522, Japan, pgs. 29.3.1-29.3.4.
PL	91	Yagishita et al., "Improvement of Threshold Voltage Deviation in Damascene Metal Gate Transistors," IEEE Transactions on Electron Devices, Vol. 48, No. 8, August 2001, pgs. 1604-1611.

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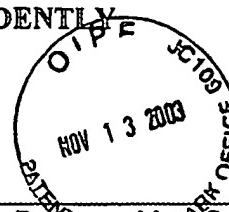
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PC	92	Yahishita et al., "High Performance Damascene Metal Gate MOSFET's for 0.1 μm Regime," IEEE Transactions on Electron Devices, Vol. 47, No. 5, May 2000, pgs. 1028-1034.
PC	93	Kimura et al., "Short-Channel-Effect-Suppressed Sub-0.1-μm Grooved-Gate MOSFET's with W Gate," IEEE Transactions on Electron Devices, Vol. 42, No. 1, January 1995, pgs. 94-100.
PC	94	Tanaka et al., "Simulation of Sub-0.1-μm MOSFET's with Completely Suppressed Short-Channel Effect," IEEE Electron Device Letters, Vol. 14, No. 8, August 1993, pgs. 396-399.
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PC	96	Sunouchi et al., "Double LDD Concave (DLC) Structure for Sub-Half Micron MOSFET," ULSI Research Center, Toshiba Corporation, 1, Komukai, Saiwai-ku, Kawasaki 210, Japan, pgs. 226-228.
PC	97	Hackler, Sr., Douglas R., "TMOS: A Novel Design for MOSFET Technology," A Thesis Presented in Partial Fulfillment of the Requirements for the Degree of Master of Science with a Major in Electrical Engineering in the College of Graduate Studies, University of Idaho, October 1999, 126 pgs.
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EXAMINER

PHAT Y. CAO

DATE CONSIDERED

3/14/05

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.